IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. An identifier indicating the status of each claim is provided.

Listing of Claims

1. (Currently Amended) A digital signal processing apparatus, comprising:

a plurality of digital signal processing blocks including at least a signal processing block for decoding and processing high speed streams of data ~~of streams~~, each of said plurality of digital signal processing blocks having a processing unit and cooperating with hardware;

a host processing block for controlling said digital processing apparatus by outputting to a respective digital signal processing block a command of a high layer, not dependent on hardware structure and not on a real time basis; and

a common bus for connecting said host processing block and said plurality of digital signal processing blocks together for transferring via said common bus both said command that is not on a real time basis and ~~for transferring~~ said high speed streams of data ~~of streams~~,

wherein said processing unit of each of said digital signal processing blocks interprets and executes said command and operates said cooperating hardware in accordance with said command~~, and~~

~~wherein said data of streams may be assigned high priority higher than said command~~.

2. (Previously Presented) The digital signal processing apparatus as set forth in claim 1,

wherein said plurality of digital signal processing blocks include at least a front end block for processing a received signal of a digital broadcast, and

wherein one of said plurality of digital signal processing blocks is a plug-in interface block for connecting external hardware.

3. - 5. (Canceled)

6. (Previously Presented) The digital signal processing apparatus as set forth in claim 1,

wherein the command is described and embedded in a script of hypertext,

wherein the hypertext is interpreted by a browser and an indication for operating a function is displayed, and

wherein a command corresponding to the function is generated.

7. (Currently Amended) The digital signal processing apparatus as set forth in claim 1,

wherein the high speed streams of data ~~of streams contains~~ contain video data and / or audio data.

8. (Original) The digital signal processing apparatus as set forth in claim 7,

wherein the video data and / or the audio data has been compressed.

9. (Currently Amended) The digital signal processing apparatus as set forth in claim 1,

wherein said bus is a general-purpose bus, and

wherein ~~each block connected to said bus~~ blocks can be added ~~or substituted~~ to said bus and a substitute for a connected block can be connected to said bus.

10. (Currently Amended) The digital signal processing apparatus as set forth in claim 9,

wherein when ~~each~~ a block ~~connected to said bus~~ is added or substituted, software for operating the added or substituted block is automatically installed.

11. (Original) The digital signal processing apparatus as set forth in claim 9,

wherein software for operating the added or substituted block is stored in a memory thereof, and

wherein when the block is added or substituted, the software stored in the memory is installed.

12. (Currently Amended) The digital signal processing apparatus as set forth in claim 9,

wherein when ~~each~~ a block ~~connected to said bus~~ is added or substituted, a service center is accessed through a telephone line, software for operating the added or

substituted block is downloaded from the service center through the telephone line, and the downloaded software is installed.

13. (Currently Amended) A digital signal processing method, comprising the steps of:

structuring functions necessary for processing a digital signal as a plurality of digital signal processing blocks and a host processing block, including at least a signal processing block for decoding and processing high speed streams of data ~~of streams~~, each of said plurality of digital signal processing blocks having a processing unit and cooperating with hardware;

connecting the host processing block and the plurality of digital signal processing blocks through a common bus; and

outputting and transferring to a respective digital signal processing block, via said common bus, a command ~~through the bus for controlling said digital signal processing apparatus, said command being~~ of a high layer, not dependent on hardware structure and not on a real time basis, for controlling said digital signal processing block;

supplying to said respective digital signal processing block, over said common bus, a high speed stream of data; and

wherein said processing unit of each of said digital signal processing blocks interprets and executes said command, operates said cooperating hardware in accordance with said command and outputs said high speed stream of data ~~of streams through the bus, and~~

~~wherein said data of streams may be assigned high priority higher than said command~~.

14. (Previously Presented) The digital signal processing method as set forth in claim 13,

wherein the plurality of digital signal processing blocks include at least a front end block for processing a received signal of a digital broadcast, and

wherein one of said plurality of digital signal processing blocks is a plug-in interface block for connecting external hardware.

15. - 17. (Canceled)

18. (Original) The digital signal processing method as set forth in claim 13, wherein the command is described and embedded in a script of hypertext.

19. (Currently Amended) The digital signal processing method as set forth in claim 13,

wherein the high speed streams of data ~~of streams contains~~ contain video data and / or audio data.

20. (Original) The digital signal processing method as set forth in claim 19, wherein the video data and / or the audio data has been compressed.

21. (Currently Amended) The digital signal processing method as set forth in claim 13,

wherein the bus is a general-purpose bus, and

wherein ~~each block connected to the bus~~ blocks can be added ~~or substituted~~ to said bus and a substitute for a connected block can be connected to said bus.

22. (Currently Amended) The digital signal processing method as set forth in claim 21,

wherein when ~~each~~ a block ~~connected to the bus~~ is added or substituted, software for operating the added or substituted block is automatically installed.

23. (Original) The digital signal processing method as set forth in claim 21,

wherein software for operating the added or substituted block is stored in a memory thereof, and

wherein when the block is added or substituted, the software stored in the memory is installed.

24. (Currently Amended) The digital signal processing method as set forth in claim 21,

wherein when ~~each~~ a block ~~connected to the bus~~ is added or substituted, a service center is accessed through a telephone line, software for operating the added or substituted block is downloaded from the service center through the telephone line, and the downloaded software is installed.

25. (Currently Amended) The digital signal processing apparatus as set forth in claim 1,

wherein said host processing block has a high level interface for processing said command; and

wherein each said plurality of digital signal processing blocks has a driver for interpreting said command, and a low level interface for controlling said hardware.